WCCF 77
64k $2500
(ssm 3800)
(32K more cost-eff.)
$750 kit

IMSAI NEWS RELEASE - For immediate release.

San Leandro, California, USA - IMSAI Manufacturing Corporation announces the world's first megabyte memory system for microcomputers. System modules offered at this time include: 65K, 32K and 16K Ram Boards controlled by IMSAI's unique Intelligent Memory Manager (IMM).

The IMSAI megabyte memory system is a complete memory system for the IMSAI 8080 and other S-100 bus computers. It consists of the RAM-16, RAM-32 and RAM-65 dynamic memory boards and intelligent memory manager (IMM) controller board. It may be implemented in a variety of configurations ranging from a single board 16K byte conventional memory to a 17-board one megabyte system with an Intelligent Memory Manager/interrupt controller. Larger multiprocessor systems may be implemented by using multiple IMSAI mainframes and the IMSAI Shared Memory Facility. Shared memory blocks can be up to 65K bytes and each processor can address up to one megabyte total of shared and local memory.

The RAM-16, RAM-32 and RAM-65 are 16K, 32K and 65K byte low power dynamic memory boards respectively. They may be used alone or in combination to form a conventional memory system of up to 65K bytes. With 400 ns access time and "hidden refresh", no wait states are required when accessed by the MPU. (One wait state may occasionally be required for refresh when accessed by some DMA controllers.) The address of each 16K byte block is individually selectable. Provision is included for read and write-protect and expansion to one megabyte when used with the IMM controller board.

The IMM is an Intelligent Memory Manager/interrupt controller board. It provides for memory expansion to one megabyte, write protect for each 1K block in the extended Space, read protection, fully vectored interrupts, "time of day" clock and real time clock.

Memory expansion is implemented by increasing the number of address lines from sixteen to twenty, and using a form of block switching to control the four added lines. The extended address space is divided into 64 16-K byte blocks of which 4 may be "on line" at any one time. The "switch" is implemented by defining a map which associates a state for address lines 16 through 19 with each state of address lines 12 through 15. The map defaults to 0000 out for all states of address lines 12 through 15 when the system is reset. It is modified and maintained under software control.

The IMM maintains a table of process control words (PCW) each of which specifies a memory configuration, memory protect mask, process entry point and system configuration flags. A PCW defines the complete system configuration for each process (user) or interrupt service routine.

System control transfers are implemented using process jumps, process calls, process returns, and interrupts. The IMM responds by automatically reconfiguring the system, saving or restoring the MPU state, and transferring program control to the proper entry or return address. A PCW stack is maintained for process nesting.

The system configuration flags are used to selectively make processes available to users under the control of the operating system. Attempts to access unavailable processes cause control to pass to the system (PCW 0).

The read write-protect function is implemented at two levels. The first level divides the extended space into 1024 1K blocks which may be write protected or enabled individually or in larger blocks, under software control or individually from front panel switches. All blocks default to the write enabled state on system reset.

The second level is a read/write protect mask which defines a segment in memory which is enabled with all other memory protected. The top and bottom of this enabled segment must fall on even 4K boundaries. The mask is switched in and out and the boundaries set under software control. The mask defaults to the "out" (no protection) state on system reset.

The first level of protection is always in effect. When the second level map is switched in, a memory location is accessable if and only if it is enabled at both levels. When an attempt is made to read to or write from a protected location, an onboard interrupt is generated. When the feature is software selected, an interrupt is also issued to the system MPU.

The interrupt control functions of the IMM are significantly more sophisticated than on typical 8080 system interrupt controllers. There are eight interrupt request lines, each with its own PCW. An interrupt, when acknowledged, is handled as a process call, and the CPU state is automatically saved. The system is automatically reconfigured to the interrupt's PCW. Returns are handled as a process return and the CPU state is automatically restored.

Interrupts can be selectively masked at the IMM. They can also be programmed to be "non-maskable" at the MPU.

The real time clock can be used to generate interrupts at Software selectable rates from 200 micro-seconds to 1600 seconds. The IMM maintains 16 4-bit nibbles which may be written or read by the system MPU. These nibbles are also multiplexed to a connector for use by an optional display. When the feature is selected, the bottom 10 nibbles are maintained as a BCD time of day clock (year/month/day/ hour/minute/second).

The "intelligence" in the IMM is implemented with an 8048 micro-computer, an 8155 memory I/O timer chip, and an 8255 ROM I/O timer chip. This provides 2K bytes of program and 320 bytes of data storage. The extended data memory stores user defined tables of configurations for read/write protect and block switching (PCW's). The interrupt vectors are stored in RAM external to the 8048 address space.

The IMM Firmware features are tailored to facilitate implementation of data acquisition, realtime processing, logging, time sharing and other systems which are likely to require very large memories. If desired, the user can specialize his system by selecting an added cost 8755 option and modifying the program.

The memory modules are offered in both assembled and kit form. Prices are as follows:

65K RAM Board Kit	-	$2,599	Assembled	-	$3,899
32K RAM Board Kit	-	$ 749	Assembled	-	$1,099
16K RAM Board Kit	-	$ 449	Assembled	-	$ 679
IMM ROM Control Kit	-	$ 299	Assembled	-	$ 399
IMM EROM Control Kit	-	$ 499	Assembled	-	$ 699

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